A Combined Power Quality Conditioner for a Dynamic Voltage Restorer Using a Novel Reference Signal Generation Method.

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Abstract -In this work a new method of reference signal generation method for the Combined Power Quality Conditioning is adopted in order to compensate both current and voltage quality issues of critical loads. The shunt converter discussed is used to eliminate distortions due to current harmonics from load side and a series converter eliminates voltage sag form the supply side. The algorithm developed algorithm for the above said controllers in order to generate a reference signal that is based on Instantaneous Reactive Power and nonlinear adaptive filter. The DC link control strategy is based upon PI controller. The proposed controller not only reduces the effects of voltage sag but also the current harmonics on the load side under distorted supply conditions. The proposed system was using simulation software MATLAB.

Index Terms -Power Quality (PQ); Reference Signal Generation; Proportional Integral (PI) controller; combined Power Quality Conditioner (CPQC).

1. INTRODUCTION

Power Quality issues are becoming more and more significant in these days because of the increasing number of power electronic devices that behave as nonlinear loads. With the increasing applications of nonlinear and electronically switched devices in distribution systems and industries, Power Quality (PQ) problems, like harmonics, flicker, imbalance so on,requires serious attention. In addition, to effect of lightening on transmission lines, capacitor banks, and various network faults can also cause PQ problems, like transients, sag as well as swell of voltage and interruption [1].

One of the best solution to compensate both current and voltage hence the power quality related problems, simultaneously, it is the use of Combined Power Quality Conditioner (CPQC) [2]. One of the electrical system adapter structures is a back to back connected inverter. The design of the back to back inverters might result in different operations in compensation accordingly. CPQC is a combination of shunt (Active Power Filter) and a series compensator (Dynamic Voltage Restorer) connected together via a common DC link capacitor, which shares the active power. The application of CPQC is to compensate the sag, swell and unbalanced voltage, as well as reactive power, current and voltage harmonics

suitable devices that could solve the problems of both consumers as well as utility. CPQC thus can help to improve as Dynamic Voltage Restorer) can

compensate for voltage sag/swell and distortion in the supply side voltage so that the voltage across a sensitive/critical load terminal is perfectly regulated [3].

A CPQC can be installed to protect the sensitive load inside the plant as well as to restrict entry of any distortion from load side. This dual functionality makes the CPQC as one of the most Control techniques play a vital role in the overall performance of the power conditioner [4]. Instantaneous power theory is generally preferred to generate reference signals for the shunt converter [2] [5]. The adaptive detection technique is used to minimize the effects of noise or parameter variation [6]. To generate reference signals simultaneously for series and shunt converter, abc-dq transform, wavelet transform [7] etc methods are adopted. DC voltage control also can be fulfilled by using proportional control and PI control [8]. The hysteresis method, space vector Pulse Width Modulation (PWM) [9] and sinusoidal PWM strategy are preferred for series and shunt side converter signal generation.

This paper presents novel contributions for CPQC control and has the following functions: The new control approach based on enhanced phase locked loop and nonlinear adaptive filter for reference signal generation is derived for series and shunt converters. A PI controller is used to control dc link voltage without any interfacing of other simulation programs.

The remainder of this paper is organized as follows. Section 2 of this paper presents a power circuit configuration of the CPQC. In sections 3, the controller algorithms of series and shunt converters are clearly presented, respectively. In section 4, the effectiveness of the proposed CPQC is tested and significant results of this paper are summarized in the conclusions.

2. POWER CIRCUIT CONFIGURATION OF CPQC

The CPQC shown in Fig.1 consists of series and shunt converter that are through connected back to back common energy storage capacitor (CDC). Dynamic Voltage Restorer (DVR) is connected through transformers between the supply and Point of Common Coupling (PCC). Active Power Filter (APF) is connected in parallel with PCC through the transformers. The main objective of DVR is to mitigate voltage sag from the source side. The filter inductor Lf and capacitor Cf are connected ac side in each phase to prevent the flow of harmonic currents generated due to switching [3]. The objective of APF is to regulate the dc link voltage between both converters and to suppress the load current harmonics [2]. The switching devices in both the converters are Insulated Gate Bipolar Transistor (IGBT) with diodes connected in anti-parallel. CDC provides the required common dc link voltage to DVR and APF.

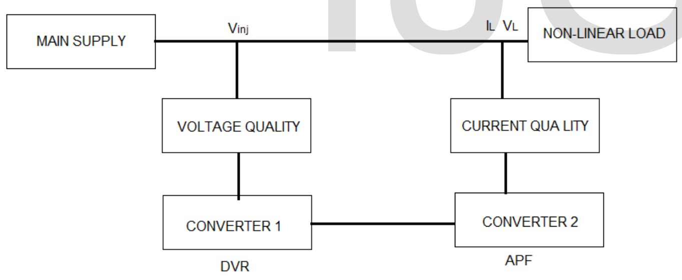


Fig.1. Schematic diagram of CPQC.

The proposed CPQC system offers two modes of operations as follows.

•DVR off and APF on: When the PCC voltage is within its operation limits, DVR is closed and APF works as the current source. APF suppress the load current harmonics and regulate dc-link voltage during this mode of operation.

• DVR on and APF on: When the PCC voltage is outside its operating range; both DVR and APF are open. DVR starts to mitigate sag using energy stored in VDC and APF continue to suppress the load current harmonics and to regulate dc link voltage.

3. CONTROL STRATEGIES OF CPQC

The control strategy of CPQC consists of APF and DVR controller. DVR controller measures the supply voltages to generate the required compensation and sag/swell detection signals. These signals are then compared in PWM controller and the required gate signals are generated. APF controller measures the load voltages, capacitor voltage, load currents and the injected current. TheAPFuses the controller algorithm for processing the measured values and to generate the required compensation signals that are then compared with hysteresis controller and the required gate signals are generated.

3.1. Control Algorithm for DVR

The control system of DVR performs voltage measurements, sag detection, reference voltage extraction and generated gate signal. Fig. 2 shows the algorithm used for control of the series converter for phase A. The control algorithm is identical for the other phases.

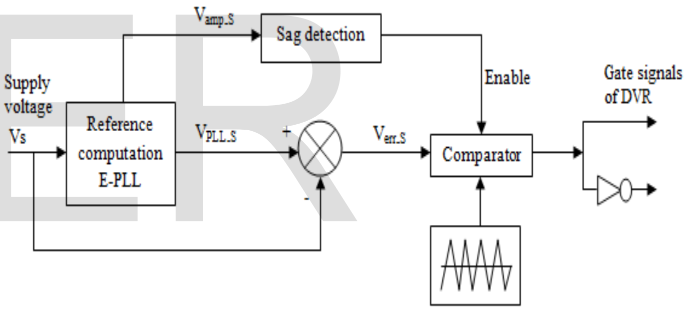


Fig. 2. Control block diagram of DVR.

Reference Signal Generation

The reference voltage computation of DVR is based on the nonlinear adaptive filter [6]. This filter can also be used as a Phase Locked Loop (PLL). The block diagram of the proposed algorithm is shown in Fig. 3. The proposed algorithm is derived from the findings of both enhanced PLL and nonlinear adaptive filter. The controller proposed in this work not only minimizes the arithmetical operands in the system but also results in reduction of complex parameter tuning. Hence to arrive at the control strategy of the DVR, the measurements of supply voltages becomes necessary.

Themeasured input signal A(t) and B(t) is input to system which receives the difference of input and the synchronized fundamental component; C(t), the amplitude of D(t); D(t), the synchronized fundamental component; E(t), PLL signal; θ(t), the phase angle of D(t).

For series inverter, A(t) corresponds to supply voltage VS and E(t) corresponds to VPLL-S. The required compensation signal Verr-s is obtained from (VPLL-S - Verr-s). C(t) corresponds to VampS and this signal is used to detect voltage sags.

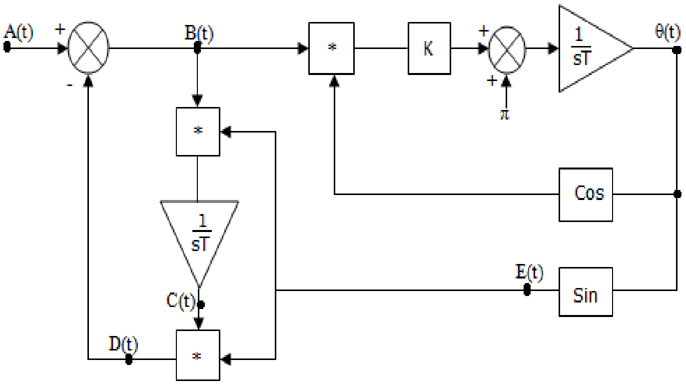


Fig. 3. Block diagram of the proposed algorithm.

Proposed Sag Detection Method

With the proposed method of fault detection, the controller can detect balanced as well as unbalanced voltage sags with almost nil error. Thus C(t) gives the magnitude of the tracked signal A(t). For example, if the amplitude of the measured Phase Ainput voltage is 220V, then 1 p.u. will be obtained for a signalC (t). If the magnitude reduces to 176V, the magnitude of the C(t) signal also falls to 0.8p.u. The voltage sag detection method is based on E-PLL method which is presented in Fig. 4. By subtracting the C(t) signal from the ideal voltage magnitude (1p.u), the voltage sag depth Sprop can be detected as shown in "Eq.(1)"

$$S_{prop} = \left|1 - C(t)\right| \tag{1}$$

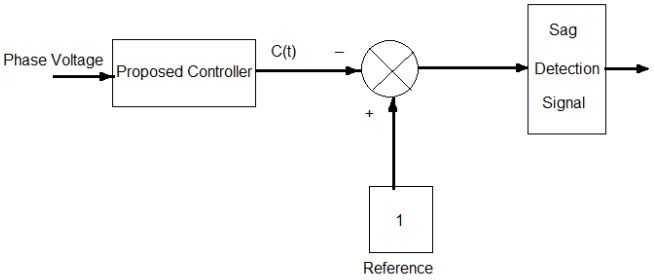


Fig. 4. Proposed sag detection method

The voltage compensation signal Verror is compared with a fixed frequency carrier wave to generate the firing pulses as PWM signals. Sine PWM control is used in order to generate the gating pulses of theDVR.

3.2. Control Algorithm for APF

The control system of APF performs reference current extraction, capacitor voltage balance control and generation of gating signals. The load voltage, voltage across capacitor, current drawn by load and injected currents are measured by APF controller. The measured values are processed by the controller algorithm of APF and it generates the required compensation signals. These signals are then compared in hysteresis controller and the required gate signals are generated. The algorithm for reference current generation is based on the Instantaneous Reactive Power Theory [10].

The control system of traditional APF is shown in Fig. 5. Three-phase load voltages, DC capacitor voltage, load currents and injected currents are the input for the control system. The capacitor voltage is controlled using PI controller.

This theory consists in the algebraic transformation of the current and voltage of the system from the abc system to αβ0 system using Clarke`s transformation as in the "Eq. (2)" and "Eq. (3)".

$$\begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & \sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \tag{2}$$

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & \sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} v_{La} \\ v_{Lb} \\ v_{Lc} \end{bmatrix} \tag{3}$$

Where ila, ilb, ilc are the load currents and Vla, Vlb, Vlc are the load voltages.

According to the p-q theory, the active, reactive and zero-sequence powers are defined as in "Eq. (4)", "Eq. (5)" and "Eq. (6)".

$$p = v_\alpha i_\alpha + v_\beta i_\beta \tag{4}$$

$$q = v_\alpha i_\beta - v_\beta i_\alpha \tag{5}$$

$$p_0 = v_0 i_0 \tag{6}$$

The currents, voltages and powers in the α-β system can be decomposed in mean and alternating values, corresponding to the fundamental and harmonic components, as in "Eq. (7)", where x can be currents, voltages and powers.

$$x = \bar{x} + \tilde{x} \tag{7}$$

Zero sequence power (p0) only exists in three-phase system with neutral wire. and are the DC and AC components of the instantaneous real power and and are the DC and AC components of the instantaneous imaginary power. The power required to be compensated by the APF are calculated as in “Eq. (8)”.

$$\begin{bmatrix} \tilde{p} \\ q \end{bmatrix} = \begin{bmatrix} \bar{v}_\alpha & \bar{v}_\beta \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \tilde{i}_\alpha \\ \tilde{i}_\beta \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ -\bar{v}_\beta & \bar{v}_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{8}$$

After adding the active power required to regulate the DC bus voltage, ploss to the alternative value of the instantaneous real power, the reference currents are calculated by “Eq. (9)”.

$$\begin{bmatrix} i_\alpha^* \\ i_\beta^* \end{bmatrix} = \frac{1}{\Delta} T \begin{bmatrix} 0 \\ \bar{q} \end{bmatrix} + \frac{1}{\Delta} T \begin{bmatrix} \tilde{p} + p_{loss} \\ \tilde{q} \end{bmatrix} \tag{9}$$

Where:

$$\Delta = \bar{v}_\alpha^2 + \bar{v}_\beta^2$$

$$T = \begin{bmatrix} \bar{v}_\alpha & -\bar{v}_\beta \\ \bar{v}_\beta & \bar{v}_\alpha \end{bmatrix}$$

The load currents are transformed from three-phase abc to αβ0 components using Clarke`s transformation, as in “Eq. (10)”.

$$\begin{bmatrix} i_a^* \\ i_b^* \\ i_c^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 & 1/\sqrt{2} \\ -1/2 & \sqrt{3}/2 & 1/\sqrt{2} \\ -1/2 & -\sqrt{3}/2 & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} i_\alpha^* \\ i_\beta^* \\ i_0^* \end{bmatrix} \tag{10}$$

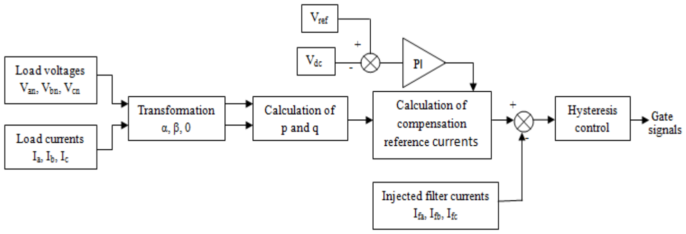


Fig. 5. Control system of traditional APF.

The most important disadvantage of IRPT theory is that increased THD content due to voltage harmonics in supply voltage and this result in incorrect reference current calculation which can cause the incorrect calculation of reference current. To overcome this problem, only one load voltage measurement is performed. With the use of the measured value which is shifted by 90° phase of virtual voltage is generated as shown in Fig. 6. This virtual voltage depends on the zero crossing point of phase-to-phase voltage of A and B phases. With the zero crossing detection, frequency compensation is made on virtual voltage. The unbalances between measured load voltages are eliminated using this control approach as in “Eq. (11)” and “Eq. (12)”.

$$V_\alpha = V_{ab} \tag{11}$$

$$V_\beta = V_{ab} \angle -90° \tag{12}$$

A PI controller is used to compensate DC link capacitor voltage if APF is in compensation state. The instantaneous active power is calculated by using the transformed values and they are applied to a 100Hz digital low pass filter.

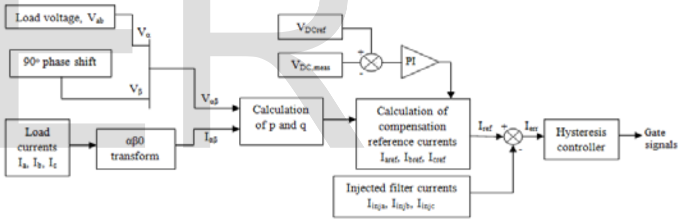


Fig. 6.Proposed APF controller.

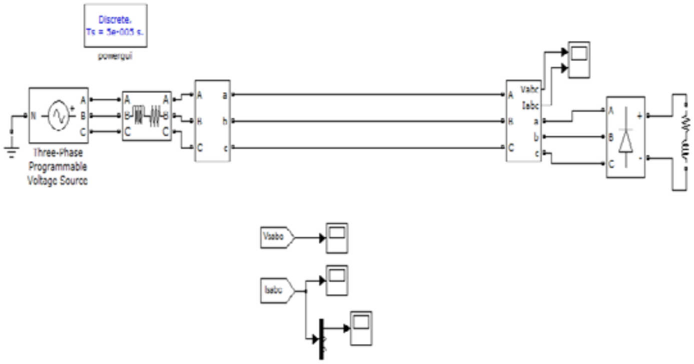
The instantaneous active and reactive currents are calculated using “Eq. (9)”. The feedback method used to control DC bus is very important. The method consists of controlling the capacitor voltage to a reference value. To achieve this, a PI control may be chosen for the error between the reference value and the capacitor voltage value at the end of each period.

$$\text{ierr} = \text{iref} - \text{if} \tag{13}$$

In the hysteresis controller, these signals are then compared and the required gate signals are generated.

4. SIMULATION RESULTS AND DISCUSSION

Simulation results of the CPQC system for power quality improvement are tested through case studies using MATLAB/SIMULINK software. This section is divided to three cases in which Case 1: nonlinear loads connected to the grid and its effect on source side. Fig.7 shows the Matlab/Simulink Model without CPQC. Universal bridge is considered as non linear load. Universal bridge diodes are considered since every power electronic device is thecause of harmonics. A three-phase diode bridge rectifier is used as a harmonic current producing load with a total harmonic distortion (THD) of 31%. Case 2: shows when DVR is off and APF is on. Fig. 13 shows the Matlab/Simulink Model of CPQC. The harmonic suppression capability of APF is analyzed. Case 3: shows when DVR is on and APF is on. The supply voltage and load voltage waveforms before and during the voltage sag are presented.



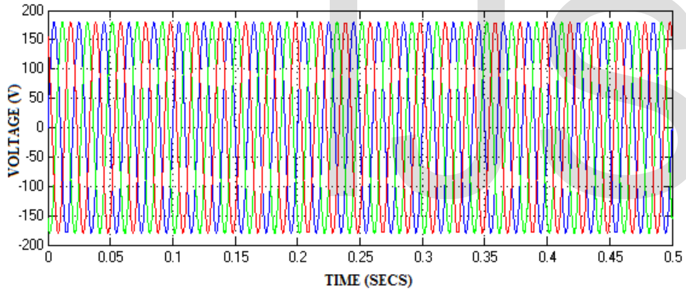


Fig. 7. Simulation results of source voltage

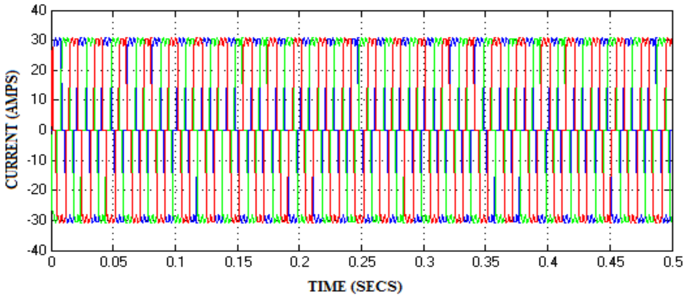


Fig. 8. source current without CPQC

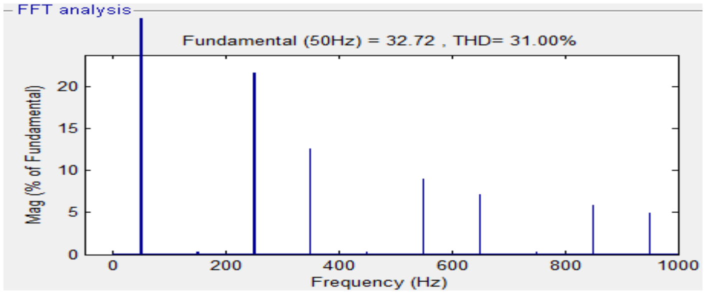


Fig. 9 Total harmonic distortion without CPQC.

Fig. 8 shows the sinusoidal source voltage and non sinusoidal source currents. Three-phase source currents are influenced by nonlinear load. Fig. 9 shows the harmonic spectrum and THD value is observed to be 31.02% of fundamental.

Fig. 10.shows how APF overcomes the load current harmonics with the proposed control algorithm. A nonlinear load current with 22% THD is approximately reduced to 3.88% with a PI controller as shown in Fig. 11.

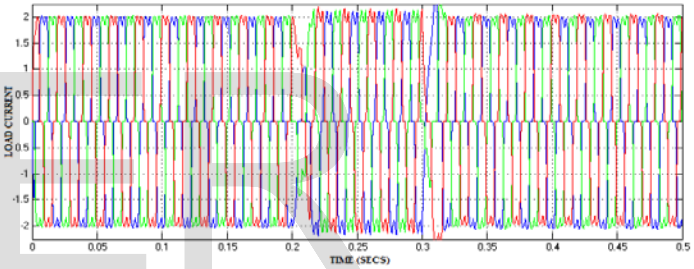


Fig. 10. Simulation results of load current with CPQC.

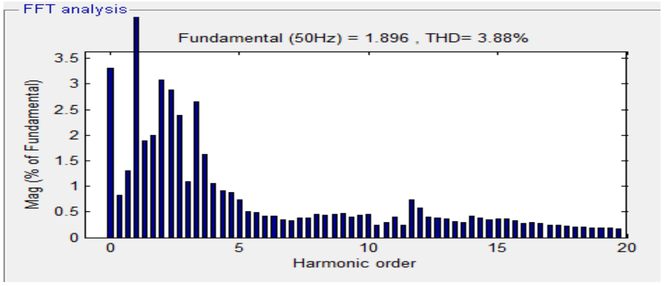
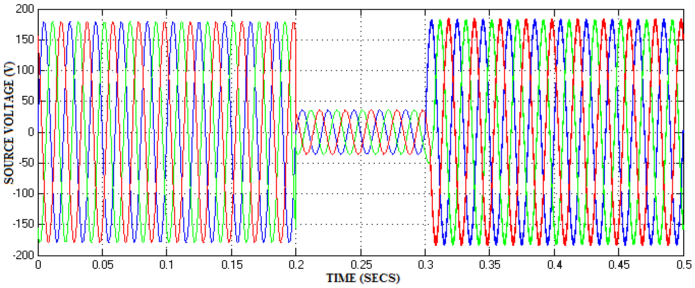
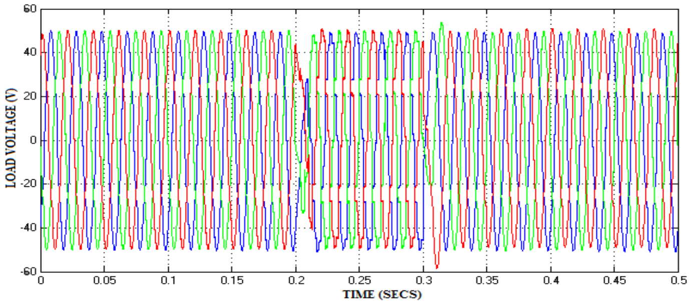


Fig. 11.Total harmonic distortion of load current.



(a)



(b)

Fig. 12.Matlab/Simulink result of (a) source voltage during sag (b) compensated source voltage

Fig. 12 shows the supply and load voltage waveforms during voltage sag, when the sag signals are applied from time period 0.2 sec to 0.3 sec. The supply current THD is approximately reduced to 5% with the PI controller

5. CONCLUSION

The Unified Power Quality Conditioner is introduced and analyzed by the controlling voltage source converter (DVR and APF) based on Enhanced PLL and nonlinear adaptive filter algorithms and dc-link voltage with a PI controller. New functionality is added to the CPQC system to quickly extract the reference signals directly for load current and supply voltage with a minimal amount of mathematical operands. The computation method is simpler than for other control algorithms of reference extraction. The number of parameters to be tuned has also beenreduced by the use of the proposed controller. The performance of the proposed CPQC and the controller for PQ improvement is tested through the case study simulations.

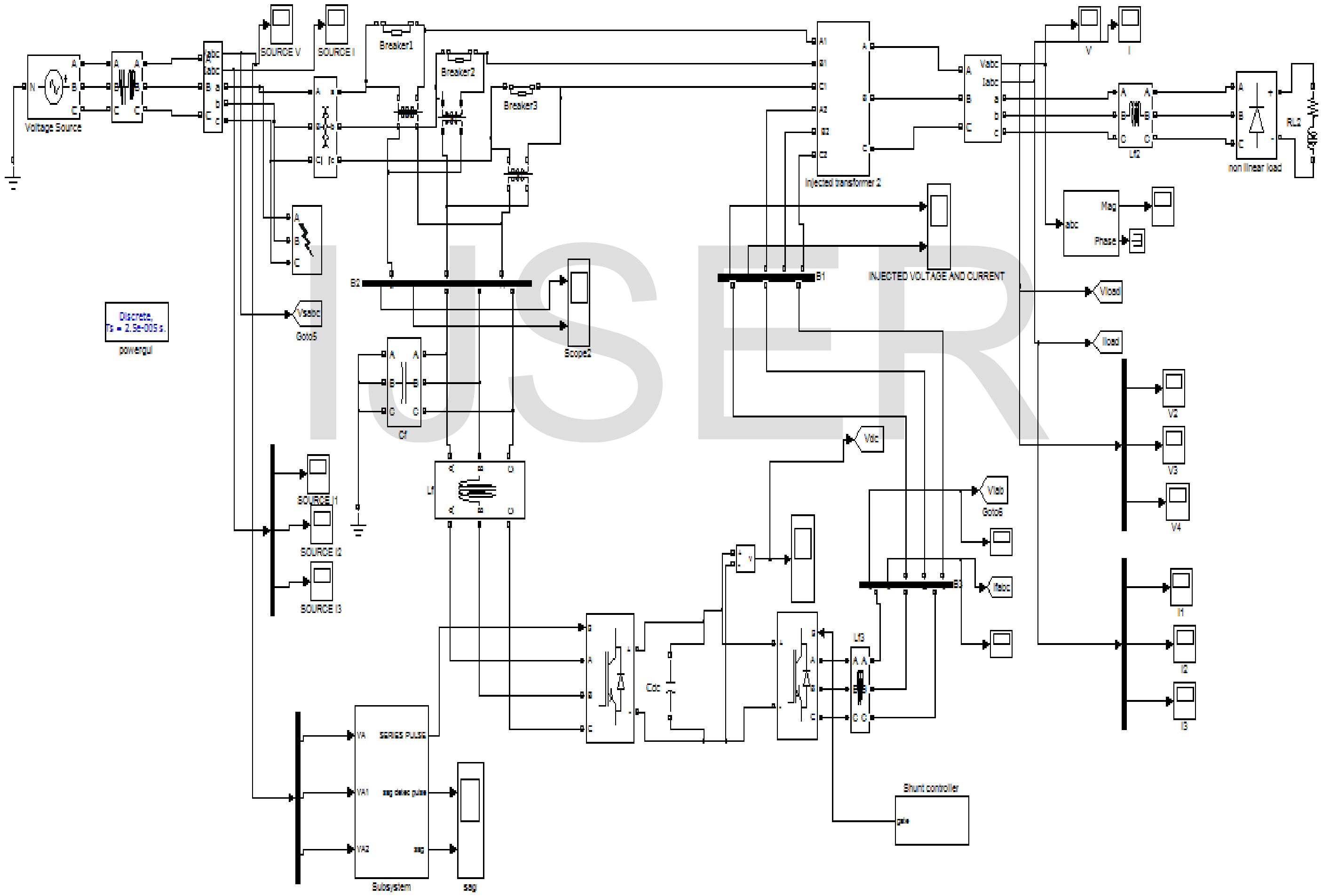


Fig. 13.Matlab/Simulink Model of CPQC

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Fig. 10.Matlab/Simulink Model of CPQC.